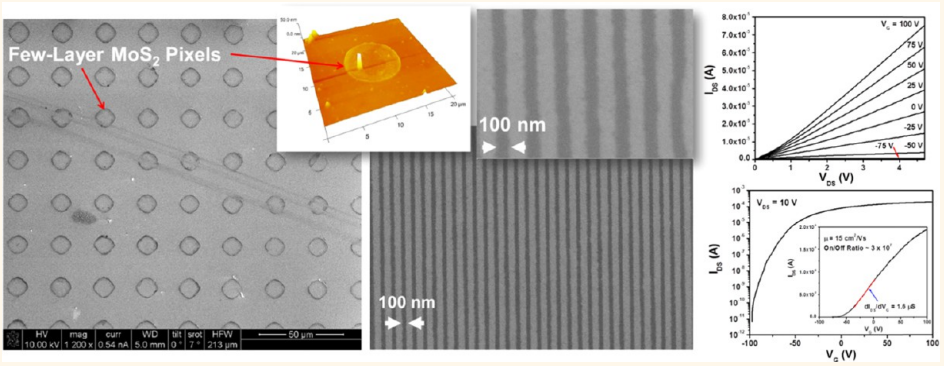
MoS_2 Transistors Fabricated *via* Plasma-Assisted Nanoprinting of Few-Layer MoS_2 Flakes into Large-Area Arrays

Hongsuk Nam,[†] Sungjin Wi,[†] Hossein Rokni, Mikai Chen, Greg Priessnitz, Wei Lu, and Xiaogan Liang*

Department of Mechanical Engineering, University of Michigan, 2011 W.E. Lay Automotive Laboratory, 1231 Beal Avenue, Ann Arbor, Michigan 48109, United States. [†]H. Nam and S. Wi contributed equally.

ABSTRACT



Large-area few-layer-MoS_2 device arrays are desirable for scale-up applications in nanoelectronics. Here we present a novel approach for producing orderly arranged, pristine few-layer MoS_2 flakes, which holds significant potential to be developed into a nanomanufacturing technology that can be scaled up. We pattern bulk MoS_2 stamps using lithographic techniques and subsequently transfer-print prepatterned MoS_2 features onto pristine and plasma-charged SiO_2 substrates. Our work successfully demonstrates the transfer printing of MoS_2 flakes into ordered arrays over cm^2-scale areas. Especially, the MoS_2 patterns printed on plasma-charged substrates feature a regular edge profile and a narrow distribution of MoS_2 flake thicknesses (*i.e.*, 3.0 $\pm$ 1.9 nm) over cm^2-scale areas. Furthermore, we experimentally show that our plasma-assisted printing process can be generally used for producing other emerging atomically layered nanostructures (*e.g.*, graphene nanoribbons). We also demonstrate working n-type transistors made from printed MoS_2 flakes that exhibit excellent properties (*e.g.*, ON/OFF current ratio 10^5—10^7, field-effect mobility on SiO_2 gate dielectrics 6 to 44 $cm^2/(V\,s)$) as well as good uniformity of such transistor parameters over a large area. Finally, with additional plasma treatment processes, we also show the feasibility of creation of p-type transistors as well as pn junctions in MoS_2 flakes. This work lays an important foundation for future scale-up nanoelectronic applications of few-layer-MoS_2 micro- and nanostructures.

KEYWORDS: nanomanufacturing · molybdenum disulfide · graphene · nanoelectronics · transistor · nanoprint

Molybdenum disulfide (MoS_2) belongs to the family of layered transition metal dichalcogenides.[1] It has been widely used as a dry lubricant and as a catalyst for desulfurization in petroleum refineries.[2] Recently, MoS_2 attracted a great deal of attention because of its attractive electronic, optoelectronic, and mechanical properties.[3−6] In the bulk form, MoS_2 is an indirect band-gap semiconductor with an energy gap of ~1.2 eV.[6] In the monolayer form, MoS_2 has a large direct band gap (~1.8 eV).[6] Therefore, MoS_2 can serve as an important complement to zero-band-gap graphene and enable new semiconductor-related applications of two-dimensional (2-D) materials such as thin-film transistors,[3,7] phototransistors,[8] chemical sensors,[9] integrated circuits,[10] and thin-film light-emitting diodes.[6,11] As a 2-D nanoelectronic material, MoS_2 is advantageous over bulk Si for suppressing the undesirable

* Address correspondence to xiaoganl@umich.edu.

Received for review March 4, 2013 and accepted June 21, 2013.

Published online June 22, 2013
10.1021/nn401093u

tunneling between drain and source regions at the scaling limit of transistors and therefore provides benefits for miniaturization of electronic devices beyond Moore's law.[12] In addition, bulk (or multilayer) MoS_2 exhibits relatively high in-plane carrier mobility comparable to that of crystalline Si,[13] as well as robust mechanical and chemical properties, which makes it an attractive material for making flexible electronic devices with high performance and long lifetime.[4,10,14]

A broad variety of prototype devices based on few-layer MoS_2, such as high-performance field effect transistors,[3,7] phototransistors,[8] sensors,[9,15] and integrated circuits,[10] have been fabricated and extensively studied in research laboratories. However, the scale-up applications of MoS_2, especially the mass production of commercially viable products, demand large arrays of orderly arranged MoS_2 structures. This requirement breaks down into two critical challenges in nanomanufacturing: (1) incorporating pristine MoS_2 films over large areas and (2) patterning MoS_2 into ordered micro- and nanostructures over large areas to obtain both desirable electronic properties and required functionality. Several approaches have been attempted to produce MoS_2 materials for large-area applications, including Scotch tape exfoliation,[3,14,16] liquid phase exfoliation in an organic solvent,[17,18] intercalation followed by forced hydration,[11,19,20] transition metal sulfurization,[21,22] thermal decomposition of thiosalts,[23] chemical vapor deposition (CVD),[24,25] van der Waals epitaxial growth,[26] *etc*. So far, a few efforts have been invested on the lithographic patterning of MoS_2 sheets and the deposition of MoS_2 crystals into ordered arrays.[27−29] All of these technologies for producing MoS_2 structures still suffer from one or more obstacles that prevent the creation of ordered, pristine MoS_2 device arrays over large areas. In particular, Scotch tape-based or liquid-phase exfoliation-based processes usually generate a poor yield of few-layer MoS_2 flakes.[3,14,16,17] Chemical intercalation methods can produce a relatively high yield of monolayer or few-layer MoS_2 flakes in colloidal solutions, but cannot arrange them into ordered arrays over large areas.[11,19,20] CVD and epitaxial methods are promising to generate very thin MoS_2 flakes over large areas in the future, but the present as-grown MoS_2 samples still feature randomly distributed micro- or nanoflakes with 10's−100's nm scale crystalline domains that are much smaller than the crystalline domains achieved in geographic MoS_2 materials (typically, 1 to 100's μm size).[1,24−26] Obviously, a nanomanufacturing technology capable of being scaled up and producing ordered and pristine few-layer MoS_2 patterns would have a transformative impact on future manufacturing of MoS_2 electronic and optoelectronic devices and systems.

In this article, we present novel transfer-printing processes for creating large-area arrays of prepatterned few-layer MoS_2 features. In this work, bulk MoS_2 films are prestructured with relief patterns by using lithographic techniques and subsequently serve as stamps for printing out MoS_2 flakes on pristine and plasma-charged SiO_2 substrates. Here, SiO_2 is chosen as the substrate material, because SiO_x-based substrates are widely used for electronic applications. Therefore, the approaches developed in this work can be generally applied to other SiO_x-based substrates such as glass, fused silica, and flexible silicone rubber. The few-layer MoS_2 flake pixels printed on such SiO_x substrates can be used to create working transistors exhibiting excellent performance. In the future, the presented printing approaches in combination with other nanolithography techniques, precise deposition and etching processes, and new high-*k* gate dielectrics can potentially be employed for producing high-performance MoS_2-based large-scale integrated circuits.

RESULTS AND DISCUSSION

Figure 1(a) schematically illustrates our approach for transfer printing prepatterned MoS_2 flakes. The fabrication process consists of the following steps. (1) The process starts with a piece of pristine bulk MoS_2. (2) Photolithography is performed to pattern a photoresist layer spin-coated on top of the MoS_2 surface. (3) Arrays of metal masks are created by depositing 100 nm Ti followed with lift-off in acetone. (4) SF_6-based reactive ion etching (RIE) is performed to transfer the Ti mask pattern onto underlying MoS_2.[29−31] (5) Ti masks are completely removed in hydrofluoric (HF) acid, and a bulk MoS_2 stamp is created. (6) A SiO_2 substrate is treated with O_2 plasma to generate electric charges on the surface.[32] (7) Finally, the bulk MoS_2 stamp is used for printing out MoS_2 flake arrays onto the SiO_2 substrate. This process can generate MoS_2 device patterns directly from pristine geographic MoS_2 materials that have the largest crystalline domains (typically, 1 to 100's μm size) and the best electronic properties to date.[1,24−26] Further, this approach can be generalized for manufacturing other emerging atomically layered nanomaterials such as graphene,[33−35] boron nitride,[36,37] and topological insulator thin films.[38] It should be noted that such a plasma-assisted transfer-printing process is significantly advantageous over voltage-based electrostatic exfoliation methods previously developed by Liang *et al*. for creating atomically layered materials,[34] in terms of application scope and printing uniformity. In particular, plasma-assisted printing can be applied to any substrates with a dielectric layer, whereas voltage-based exfoliation processes can only be used for conductive substrates. Furthermore, plasma-induced surface charges are usually immobilized and uniformly distributed over dielectric substrates and, therefore, result in uniform attractive stress for printing MoS_2 features over large areas. However, voltage-generated free charges are movable in the conductive substrate, and they tend to accumulate at locations with the

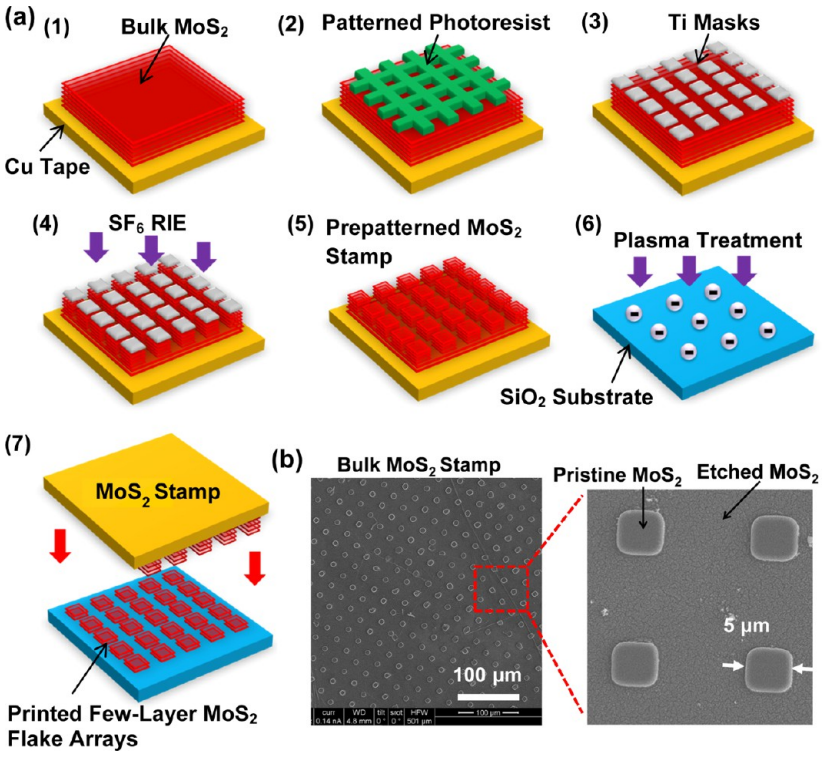


Figure 1. (a) Schematic flowchart of transfer printing of prepatterned few-layer MoS_2 flakes, which includes (1) initial bulk MoS_2 with a pristine surface; (2) photolithography for patterning device features; (3) formation of Ti masks by metal deposition followed by lift-off; (4) plasma etching of underlying MoS_2; (5) removal of Ti masks and finalization of a bulk MoS_2 stamp bearing relief features; (6) plasma treatment of the SiO_2 substrate; (7) direct transfer printing of prepatterned few-layer MoS_2 flakes onto the substrate. (b) SEM images of a bulk MoS_2 stamp prestructured with 5 μm size periodic pillars.

smallest stamp/substrate gap, resulting in nonuniform electrostatic printing stress and a high risk of electrical leakage.[34]

Figure 1(b) shows scanning electron micrographs (SEMs) of an exemplary MoS_2 stamp prepatterned with 5 μm size, 600 nm high pillars. The fabrication detail is described in the Methods and Materials section. The zoomed view in Figure 1(b) shows that the SF_6 plasma-etched area exhibits a relatively high roughness, which is attributed to plasma etching or ion bombardment. However, the raised pillar mesas protected by the Ti masks are still as smooth as a pristine MoS_2 surface. This should yield a conformal contact with the flat substrate during a mechanical printing process and therefore a high transfer-printing efficiency of MoS_2 flakes.

The details of the transfer-printing process are described in the Methods and Materials section. Figure 2(a) and Figure S1 in the Supporting Information display SEM images of MoS_2 flakes printed on a pristine SiO_2 surface. These images, captured over a large printed area (~1 cm^2), show that the mechanical printing process can produce large-area, orderly paved arrays of MoS_2 pixel features. However, most of the printed pixels have relatively irregular edge profiles that are not faithfully correlated to the edge profiles of pillars prestructured on the bulk stamp.

The thickness data of MoS_2 pixels were obtained by using an atomic force microscope (AFM). For each of the printed MoS_2 pixels, the average flake thickness was extracted from AFM topographic data. Figure 2(b) plots the statistical distribution of the average thickness data of 100 MoS_2 flake pixels of 10 μm size produced in a single transfer-printing cycle. Figure 2(b) shows that the overall average flake thickness is measured to be 4.1 nm (~6 monolayers), and the standard deviation is 2.2 nm (~3 monolayers) over a ~1 cm^2 area. About 95% and 80% of printed MoS_2 flakes are thinner than 10 and 5 nm, respectively.

Figure 3(a) shows an SEM image of MoS_2 patterns printed onto an O_2 plasma-charged SiO_2 substrate. Figure S2 in the Supporting Information lists more SEM images of MoS_2 patterns with various dimension sizes, which were captured from different locations over the printed area. These images show that the printing process on plasma-charged substrates can produce large-area, orderly arranged arrays of MoS_2 flake pixels with a higher uniformity of pixel profiles in comparison with the printing result on a pristine substrate. In particular, MoS_2 pixel patterns feature clear, well-defined edge profiles that are faithfully correlated to the edge profiles of pillars prestructured on the bulk stamp. The zoomed image in Figure 3(b) reveals that the clear edge profile of a MoS_2 pixel is indeed made up of a ring-shaped MoS_2 ribbon. Such outer edge ribbons of MoS_2 pixels have widths ranging from 200 to 400 nm. Besides these edge ribbon features, there are indeed

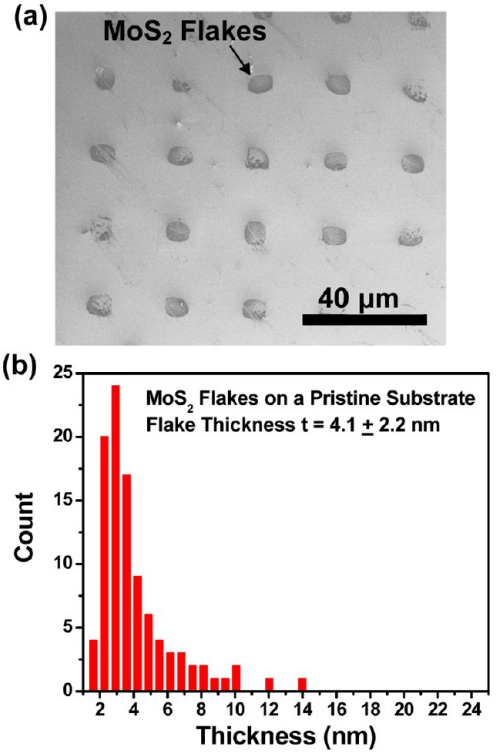


Figure 2. (a) SEM image of arrays of 10 μm size MoS_2 flake pixels printed onto a pristine SiO_2 substrate. (b) Stacked column chart of the average thickness data collected from 100 as-printed MoS_2 pixels. The thickness data were obtained from MoS_2 pixels printed over a ~1 cm^2 area by using an AFM.

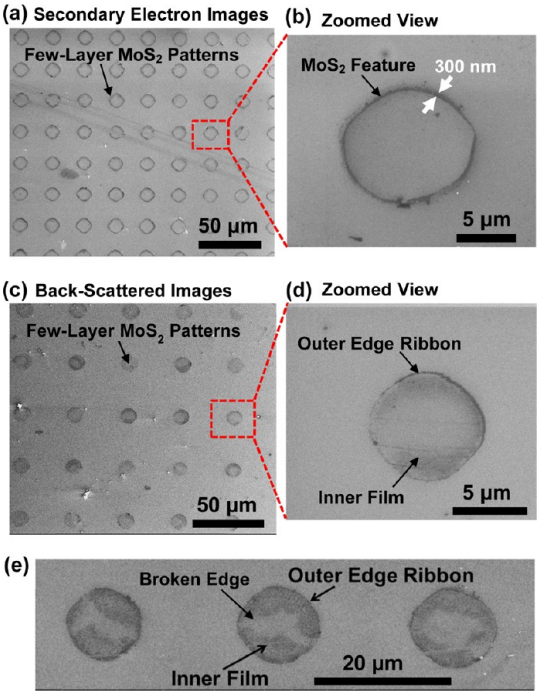


Figure 3. (a, b) Secondary-electron SEM images of MoS_2 pixel arrays printed onto an O_2 plasma-charged substrate, which exhibit clear, well-defined edge profiles faithfully correlated to the edge profiles of pillar features on the bulk MoS_2 stamps. (c, d) Backscattered SEM images of MoS_2 pixel arrays, which show the presence of thin inner MoS_2 flakes within each printed pixel. (e) Backscattered image of MoS_2 pixels with broken inner films.

thinner MoS_2 films or flakes located in the inner regions of printed pixels enclosed by the edge ribbons. These inner MoS_2 flakes typically exhibit a poor feature contrast in secondary-electron images. To enhance the SEM contrast, printed MoS_2 pixels were also imaged by detecting backscattered electrons (BSEs), as shown in Figure 3(c–e), which are often used to detect contrast between areas with different chemical compositions. The BSE image contrast in Figure 3(c–e) suggests the presence of thin MoS_2 flakes within each of the pixels. X-ray energy dispersive spectrometer (EDS) spectra were captured from the edge ribbons as well as the inner films of MoS_2 pixels, as shown in Figure S3 (see the Supporting Information). The EDS results confirm the presence of sulfur and molybdenum in both the edge and inner portions of printed pixels. In addition, Figure S4 in the Supporting Information displays optical micrographs of printed MoS_2 pixels on a 330 nm thick SiO_2 substrate, and the feature contrast further confirms the presence of inner flakes within printed MoS_2 pixels. The spatial variation of BSE image contrast and the EDS intensity of MoS_2-associated peaks suggest an interpixel variation of MoS_2 flake thickness over the printed substrate. To obtain the inner flake thickness data, MoS_2 pixels with partially broken inner films (*e.g.*, the pixels shown in Figure 3(e) and Figure S4(c)) were imaged by using AFM, and the thickness of an inner MoS_2 flake was measured from its broken edges.

Figure 4(a) displays an AFM image of an exemplary MoS_2 pixel consisting of a relatively thick edge ribbon and broken inner flakes. The scan line denoted by the solid line and accordingly plotted in Figure 4(b) explicitly displays that the thickness values measured at the left and the right sides of this outer edge ribbon are 7 nm (~11 monolayers) and 8 nm (~12 monolayers), respectively; the thickness of the broken inner flakes is measured to be 2.4 nm (~4 monolayers). The thickness data acquired from 10 scan lines are used to calculate the average thickness of the inner film and the outer edge ribbon of an individual MoS_2 pixel. Figure 4(c) plots the statistical distribution of the average thickness data of 100 MoS_2 pixels printed on a plasma-charged substrate. Here, the thickness data of inner films (solid columns) and outer edge ribbons (blue hatched columns) of MoS_2 pixels are separately plotted. Figure 4(c) shows that the overall average thickness of outer edge ribbons is 17 nm (~26 monolayers) with a standard deviation of 3 nm (~5 monolayers), whereas the overall average thickness of inner films is 3.0 nm (~5 monolayers) with a standard deviation of 1.9 nm (~3 monolayers). About 90% of inner flakes of MoS_2 pixels printed on a plasma-charged SiO_2 substrate are thinner than 5 nm (~8 monolayers). On the basis of such SEM, AFM, EDS, and optical micrograph characterizations, it is concluded that microscale MoS_2 pixels printed on a plasma-charged SiO_2 surface feature

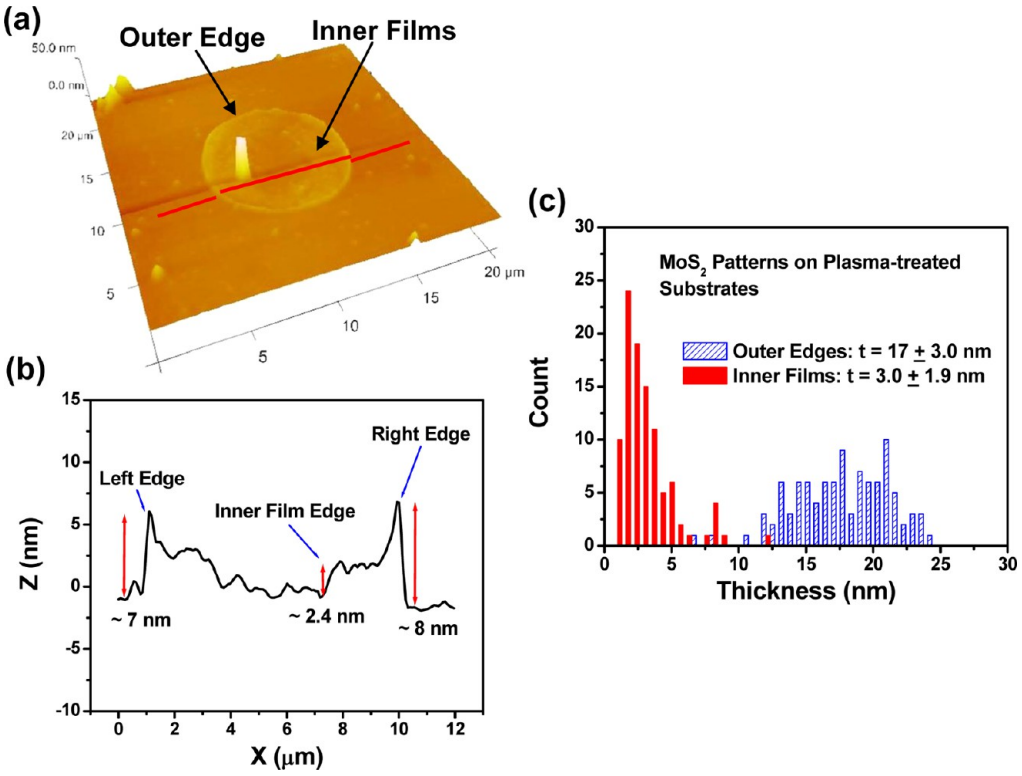


Figure 4. (a) AFM image of a 10 μm size MoS_2 pixel printed on a plasma-charged SiO_2 substrate. The solid line indicates a scanning trace across the pixel, which is explicitly plotted in (b). (c) Stacked column chart of the average thickness data collected from 100 as-printed MoS_2 pixels. Here, the thickness data acquired from the inner flakes (solid columns) and the outer edge ribbons (hatched columns) of these MoS_2 pixels are separately plotted.

relatively thinner inner films or flakes enclosed by relatively thicker ring-shaped edge ribbons and a higher percentage yield of few-layer MoS_2 flakes thinner than 5 nm in comparison with pixels printed on a pristine SiO_2 substrate.

To obtain a preliminary understanding of plasma-assisted printing mechanisms responsible for the resultant morphology of MoS_2 pixels, Maxwell stress tensor calculation was performed and used for evaluating the distribution of surface charge-induced electrostatic attractive stress between the bulk MoS_2 stamp and the dielectric substrate.[39,40] Figure 5(a) illustrates the 2-D model for the calculation, in which a plasma-charged SiO_2 substrate is in contact with a bulk MoS_2 stamp and the surface charge density is arbitrarily set to 0.05 C/m^2 (currently we lack experimentally measured data of surface charge densities). Figure 5(b) plots the calculated attractive stress exerted by the plasma-charged SiO_2 substrate on the bulk MoS_2 stamp as a function of positions. Figure 5(c) shows the zoomed view of the attractive stress distribution within a single MoS_2 mesa in contact with a SiO_2 surface. It is found that the attractive stress acting on a microscale MoS_2 mesa is uniform in the central region of the mesa but is significantly increased along the mesa edges due to the fringe effect. During a transfer-printing process, such high attractive stress at the mesa edges is expected to result in the exfoliation of MoS_2 flake pixels with well-defined edges, as experimentally demonstrated. In addition, the strong electric field at the MoS_2/SiO_2 interface is expected to influence dispersion and dipole interactions of atoms there and therefore change the cohesive energy of MoS_2 layers close to the SiO_2 surface.[41,42] This could lead to a dependence of the number of printed MoS_2 monolayers on the field magnitude, which could qualitatively explain our experimental result that for MoS_2 pixels printed on plasma-charged substrates the edge portions are statistically thicker than the inner flakes, as shown in Figure 4(c). Our future theoretical simulation work will incorporate quantum mechanics, molecular simulations, and experimentally measured surface charge data to quantitatively analyze the effects of electric field on the number of printed MoS_2 monolayers.

Although plasma-assisted printing can produce large-area arrays of microscale MoS_2 pixels with regular edge profiles, many pixels have broken areas in their central regions, as shown in Figure 3(e) and Figure S4(c). This can be attributed to several possible reasons, including the limited size of crystalline domains in bulk MoS_2, nonuniformity of attractive stress within a microscale MoS_2 pixel mesa, as discussed in the simulation analysis, and the paradigm rule that the direct exfoliation of a large-area atomic layer (*e.g.*, a complete microscale MoS_2 pixel film free of defects) is thermodynamically unfavorable.[43,44] Such an analysis

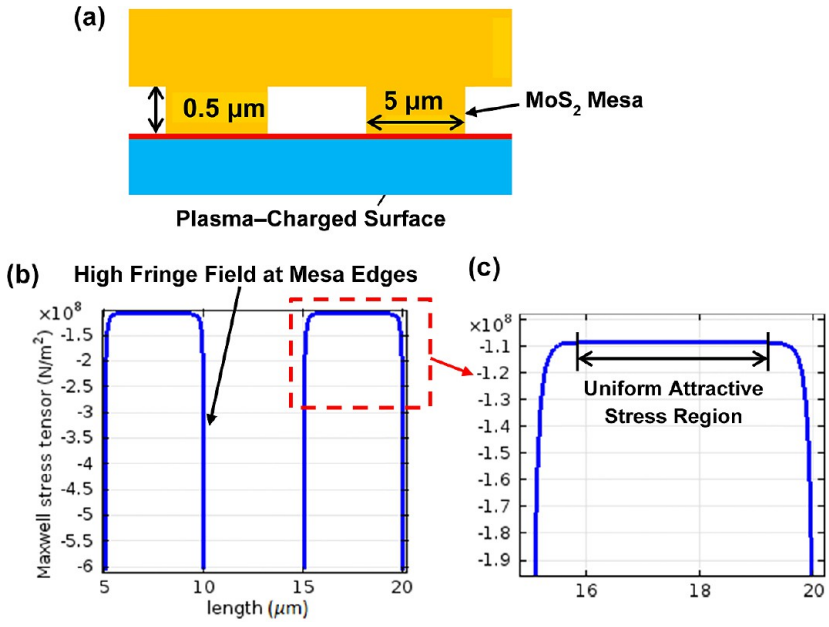


Figure 5. (a) Illustration of the 2-D model for Maxwell stress tensor calculation of surface charge-induced electrostatic attractive stress between the bulk MoS_2 stamp and the dielectric substrate. (b) Calculated attractive stress plotted as a function of positions. (c) Zoomed view of attractive stress distribution within a single MoS_2 mesa in contact with a SiO_2 surface. It is found that the attractive stress acting on a microscale MoS_2 mesa is uniform in the central region of the MoS_2 mesa but is significantly increased along the mesa edges due to the fringe effect.

suggests that it is indeed desirable to prepattern bulk MoS_2 stamps with densely arranged nanostructures that can improve the printing fidelity and eliminate the defects in the middle of printed patterns. In addition, such relief nanostructures are expected to generate a higher fringe field during printing processes because of the higher density of sharp feature edges and result in the higher transfer-printing efficiency of MoS_2 features. So far we have not developed a scalable process for patterning nanostructures on bulk MoS_2 because of its overly rough surface. However, we and other groups have successfully realized the nanopatterning of highly oriented pyrolytic graphite (HOPG) stamps with 100 nm half-pitch gratings using nanoimprint lithography, as shown in Figure 6(a).[45,46] The fabrication of HOPG stamps is described in the Methods and Materials section. Figure 6(b) shows SEM images of 100 nm half-pitch graphene nanoribbons (GNRs) produced by using plasma-assisted transfer printing. The printed GNRs exhibit a high degree of uniformity in ribbon widths over large areas and do not exhibit any visible defects in the middle of individual ribbons. The thickness of GNRs was measured to be 2.0 ± 1.0 nm by using an AFM. This work demonstrates that (1) nanoscale defect-free atomic layer patterns can be more easily produced by using plasma-assisted printing in comparison with microscale ones; (2) plasma-assisted printing can be generalized for producing high-quality nanostructures of other atomically layered materials.

To evaluate the electronic properties of printed MoS_2 flakes, we fabricated field-effect transistors (FETs) using MoS_2 pixels printed on plasma-charged SiO_2/p^+ Si substrates. The FET fabrication details are described in the Methods and Materials section. Figure 7(a) shows a BSE image of an inner flake of a MoS_2 pixel that was used to fabricate a back-gated FET with flake thickness of ~5 nm, channel length of $L = 5.4$ μm, average channel width of $W \approx 3.7$ μm, and gate dielectric thickness of $d = 330$ nm. Figure 7(b) plots drain−source current (I_{DS}) *versus* drain−source voltage (V_{DS}) characteristics of this exemplary FET under different gate voltages (V_G) ranging from −75 to 100 V. Figure 7(c) plots the $I_{DS}-V_G$ characteristics under a fixed drain−source voltage ($V_{DS} = 10$ V). As shown in Figure 7(b,c), this FET exhibits n-type conduction with an ON/OFF current ratio (I_{ON}/I_{OFF}) of ~10^7. The transconductance at the linear region of the $I_{DS} - V_G$ characteristic curve was obtained as $dI_{DS}/dV_G = 1.60$ μS by the linear fitting (denoted with the red solid line in the inset of Figure 7(c)). The field-effect mobility was estimated to be $\mu = 22$ cm^2/(V s) by using eq 1 (valid for the linear region of MoS_2-based FETs with microscale channel widths), where ε_0 is the vacuum permittivity, $\varepsilon_r \approx 3.9$ is the dielectric constant of SiO_2, C_{ox} is the gate capacitance, and W/L is the width/length ratio of the MoS_2 flake channel. The field-effect mobility values obtained from other FETs made from the inner flakes of printed MoS_2 pixels range from 6 to 44 cm^2/(V s), which are comparable to the highest mobility values previously reported for MoS_2 FETs using SiO_2 as the gate dielectric.[14,47] This indicates that our transfer-printing approaches can produce high-quality MoS_2 features and are suitable for practical nanoelectronic

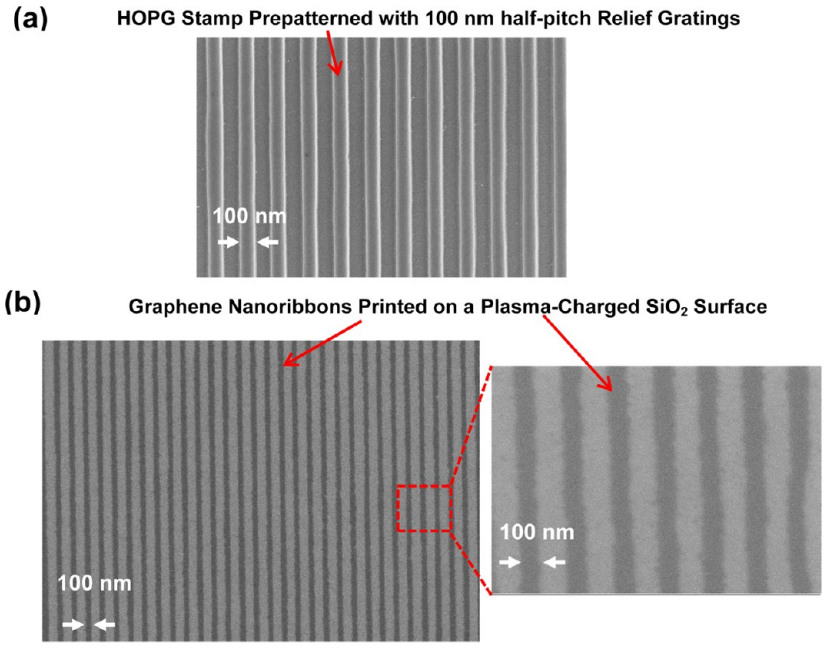


Figure 6. SEM images of (a) a HOPG stamp prepatterned with 100 nm half-pitch relief gratings by using nanoimprint lithography followed with plasma etching and (b) graphene nanoribbons printed onto a plasma-charged SiO_2 substrate.

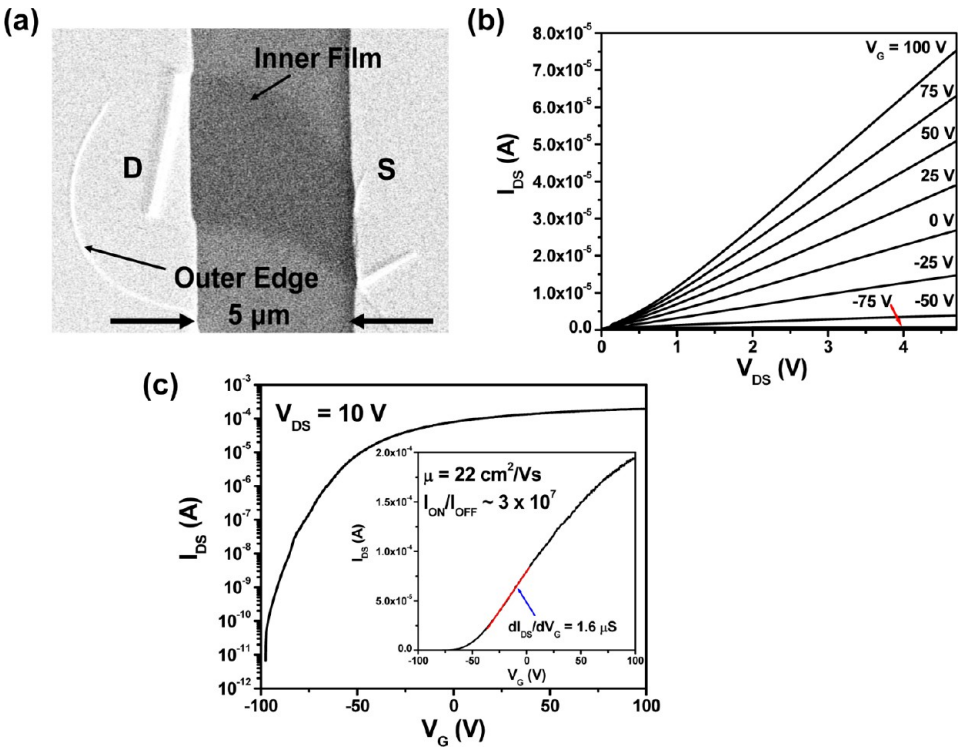


Figure 7. (a) BSE image of an exemplary back-gated FET made from the inner flake of a printed MoS_2 pixel with flake thickness of ~5 nm, channel width of ~3.7 μm, channel length of ~5.4 μm, and gate dielectric (SiO_2) thickness of 330 nm, in which Ti/Au contacts were deposited as drain (D) and source (S) contacts and the p^+ silicon substrate serves as a back gate. (b) $I_{DS}-V_{DS}$ characteristics under different gate voltages (V_G) ranging from −75 to 100 V. (c) Semilogarithmic plot of an $I_{DS}-V_G$ characteristic curve under a fixed drain−source voltage V_{DS} = 10 V, which exhibits an ON/OFF current ratio (I_{ON}/I_{OFF}) ≈ 10^7. The inset graph shows the linear plot of the same $I_{DS}-V_G$ curve, and the transconductance (dI_{DS}/dV_G) is obtained by fitting the linear region of the $I_{DS}-V_G$ curve, as indicated by the red line. The field-effect mobility is subsequently extracted to be μ = 22 $cm^2/(V\ s)$ for this FET.

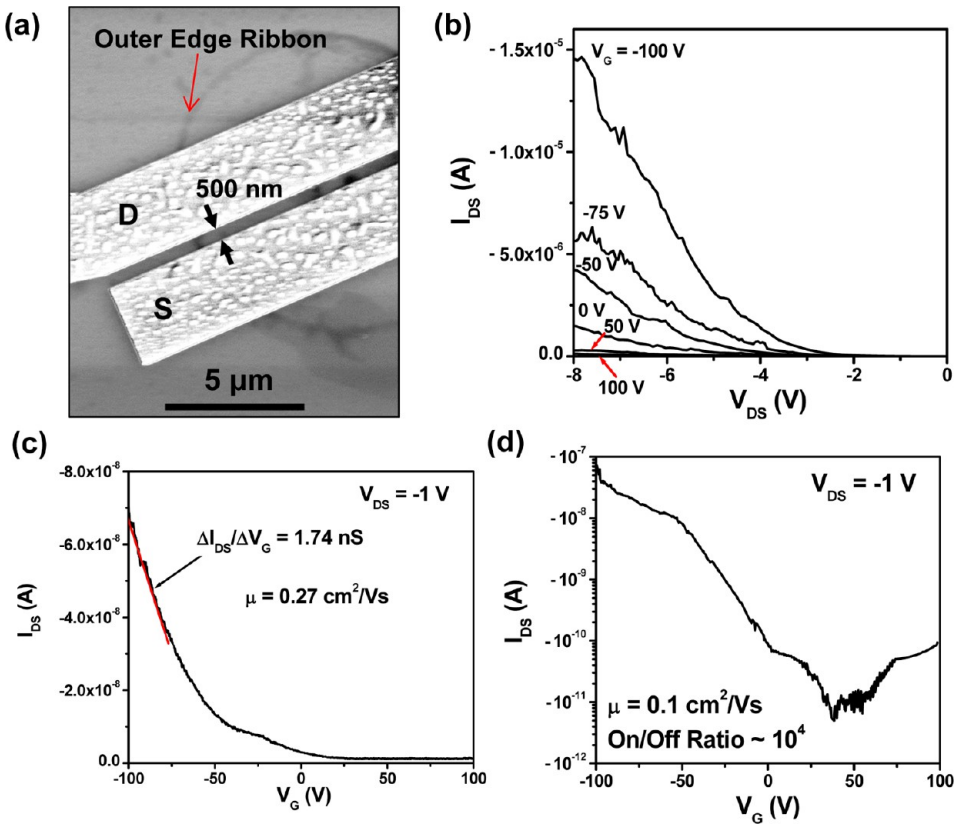


Figure 8. (a) SEM image of an exemplary back-gated FET made from the outer edge ribbon of a printed MoS_2 pixel with channel width of ~300 nm, channel length of ~500 nm, and gate dielectric (SiO_2) thickness of 330 nm. $I_{DS}-V_{DS}$ (b) and $I_{DS}-V_G$ (c) characteristics of this edge ribbon-based FET exhibit p-type conduction and field-effect mobility of ~0.27 cm^2/(V s). (d) $I_{DS}-V_G$ characteristics of a p-type FET made from a MoS_2 flake blank-treated by SF_6 plasma.

applications.

$$\mu = \frac{1}{C_{ox}\frac{W}{L}V_{DS}}\left(\frac{dI_{DS}}{dV_G}\right) \qquad C_{ox} = \frac{\varepsilon_0\varepsilon_r}{d} \qquad (1)$$

We also fabricated FETs using the ring-shaped edge ribbons of MoS_2 pixels as the semiconducting channels. To make an edge ribbon-based FET, electron-beam lithography (EBL) followed by metal evaporation and lift-off was performed to fabricate drain and source electrodes precisely aligned to the specific segment of the edge ribbon of a MoS_2 pixel. In EBL, the overlay alignment was carefully performed to avoid incorporating any inner pixel flakes into the FET channel. Figure 8(a) shows an SEM image of an exemplary edge ribbon-based FET with a channel width of $W \approx 300$ nm, channel length of $L \approx 500$ nm, and average MoS_2 thickness of ~10 nm. Figure 8(b,c) displays $I_{DS}-V_{DS}$ and $I_{DS}-V_G$ characteristics, respectively, which show that this edge ribbon-based FET exhibits p-type conduction for $V_G = -100$ to 100 V. The transconductance at the linear region of the $I_{DS}-V_G$ characteristic curve was obtained as $dI_{DS}/dV_G = -1.74$ nS by the linear fitting (denoted with the red solid line in the inset of Figure 8(c)). The field-effect mobility was estimated to be $\mu = 0.27$ cm^2/(V s) by using eq 2, where C_g is the average gate capacitance associated with a single MoS_2 edge ribbon per unit channel length [unit: F/m]. Here, C_g is calculated by using a simulation model based on finite element analysis that takes into account the fringe effect at the MoS_2 nanoribbon edges, as shown in Figure S5 in the Supporting Information. Such a fringe effect can significantly affect the values of C_g for MoS_2 FETs with nanoscale channel widths. The field-effect mobility values measured from other edge ribbon-based FETs range from 0.1 to 1.0 cm^2/(V s).

The p-type conduction is generally observed in other edge ribbon-based FETs, and it is attributed to the chemical doping to the edge portions of MoS_2 pixels, which might be induced during the SF_6 RIE process for patterning pillars in bulk MoS_2 stamps. To further identify such a plasma-induced doping mechanism, a pristine 10 μm size MoS_2 flake with initial thickness of ~20 nm was blank-etched by SF_6 plasma. After etching, the flake thickness was reduced to ~10 nm. The FET made from this flake also exhibits p-type conduction, as shown in Figure 8(d). The field-effect mobility is extracted to be ~0.1 cm^2/(V s), which is consistent with the mobility values measured from edge ribbon-based FETs. This test verifies that the p-type conduction is indeed caused by the plasma-induced doping. This also provides a simple method for making p-type MoS_2 FETs and rectifying diodes. For example, an n-type FET made from a 40 nm thick MoS_2

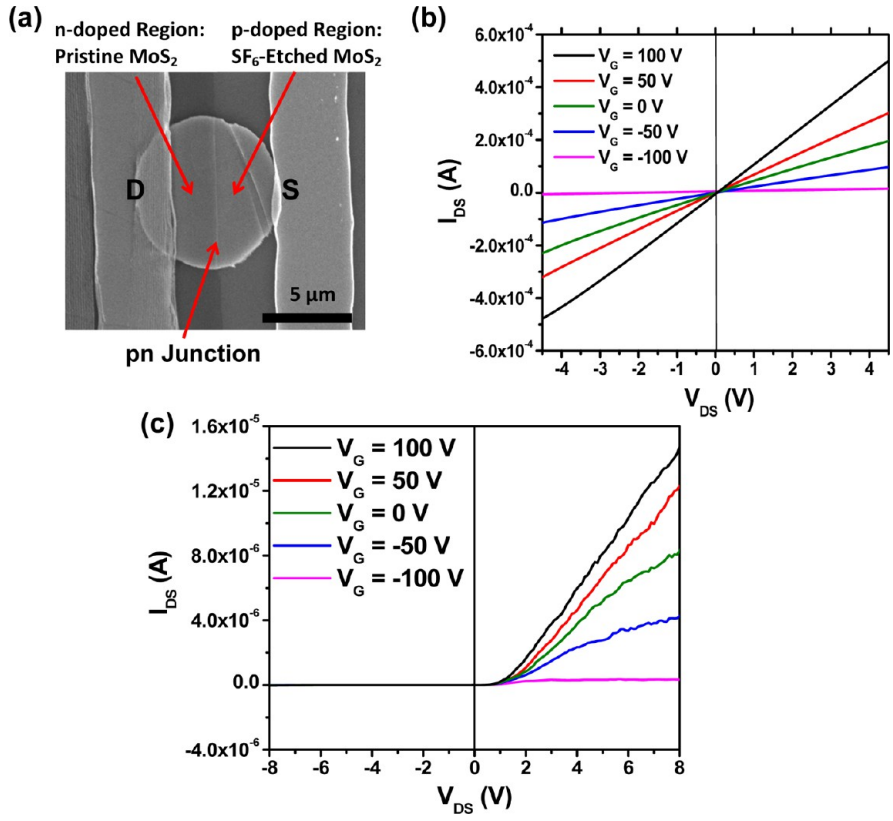


Figure 9. (a) SEM image of a pn junction formed by the partial etching of a MoS_2 pixel using SF_6-based plasma. (b) $I_{DS}-V_{DS}$ characteristic curves of the MoS_2 pixel FET under various gate voltages measured before the SF_6 plasma etching, which exhibit a linear and symmetric transport property independent of the polarity of V_{DS}. (c) $I_{DS}-V_{DS}$ curves measured after the plasma etching, which show a strong rectification of the drain−source current.

pixel was partially etched with SF_6 plasma in selected areas to form a p-doped region (*i.e.*, the etched region with the final MoS_2 thickness of ~20 nm) adjacent to the n-doped region (*i.e.*, the pristine region protected by a patterned photoresist layer), as shown in Figure 9(a). Figure 9(b,c) show the $I_{DS}-V_{DS}$ characteristics of this FET measured before and after the plasma etching, respectively. Before etching, the FET exhibits linear and symmetric $I_{DS}-V_{DS}$ characteristics independent of the polarity of V_{DS}, whereas after etching it exhibits a strong rectification of the drain−source current. This indicates the formation of a pn junction in the MoS_2 pixel. Further research will be performed to precisely control the doping profile in MoS_2 features and enable new device applications.

$$\mu = \frac{L}{C_g V_{DS}} \left(\frac{dI_{DS}}{dV_G}\right) \quad (2)$$

Our current printing approaches can generate few-layer MoS_2 flakes with the change of thickness mainly in the range 0.7−10 nm on a pristine SiO_2 substrate (Figure 2(b)) or 0.7−5 nm on a plasma-charged substrate (Figure 4(c)). As-printed MoS_2 pixels with such flake thickness distributions over large areas are still suitable for scale-up transistor-based electronic applications (if not for all applications), because previous works have demonstrated that FETs made from multilayer MoS_2 flakes with thicknesses ranging from 2 to 50 nm exhibit excellent and stable transport properties (*i.e.*, high ON/OFF ratios ranging from 10^4 to 10^7, high field-effect mobility values on the order of 10s $cm^2/(V\ s)$ on SiO_2-based dielectrics and 100's $cm^2/(V\ s)$ on high-*k* dielectrics, as well as subthreshold slopes of 60−70 mV/decade for top-gated FETs).[48−50]

To evaluate the potential scalability of our printing approaches especially for future scale-up transistor-based applications, we investigated the uniformity of the transport characteristics of MoS_2 FETs produced by plasma-assisted printing as well as the dependence of FET characteristics on the change of the MoS_2 thickness. Figure S6 in the Supporting Information shows the transport characteristics of 14 FETs produced in a single printing cycle. Figure 10 displays (a) ON/OFF current ratio and (b) field-effect mobility data measured from these FETs, which are plotted as a function of the MoS_2 thickness. These FETs have different flake thicknesses ranging from 3 to 20 nm. It should be noted that although the thickness values of most as-printed MoS_2 flakes can be controlled to be less than 10 nm, as shown in Figures 2(b) and 4(c), relatively thicker flakes (*i.e.*, thickness ~10−20 nm) were intentionally chosen for making FETs in order to extend the investigation range of the flake thickness values and analyze the degree of redundancy in the control of the MoS_2 thickness. Figure 10 shows that in spite of the variation of the MoS_2 flake thickness in the range

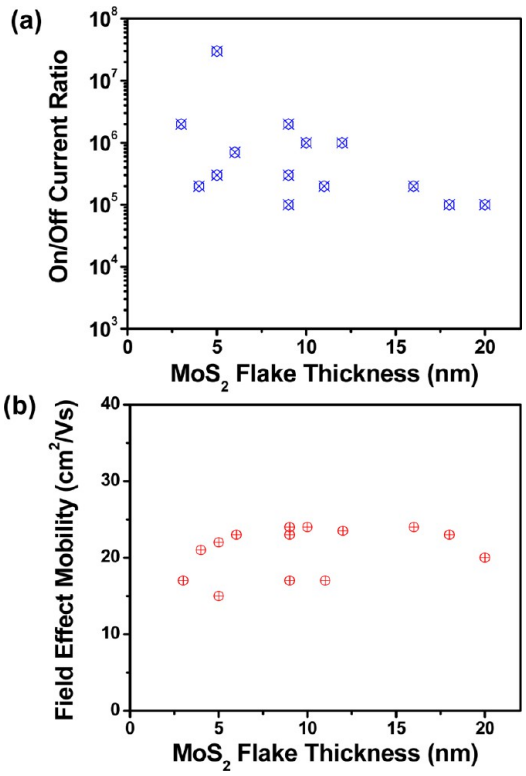


Figure 10. (a) ON/OFF current ratio and (b) field-effect mobility data extracted from the FET characteristics listed in Figure S6, which are plotted as a function of the MoS_2 flake thickness.

3−20 nm, all the FETs exhibit high ON/OFF ratios in the range 10^5−10^7, reasonably high field-effect mobility values on SiO_2 gate dielectrics ranging from 15 to 24 cm^2/(V s), and uniform threshold gate voltages around $V_{th} \approx -50$ V. Such results preliminarily demonstrate that the MoS_2 FETs produced by plasma-assisted printing do not exhibit a sensitive dependence of FET characteristics on the change of the MoS_2 thickness in the range 3−20 nm. This also suggests that our printing approaches can generate a high yield of electronic-grade MoS_2 flakes with an acceptable degree of uniformity in FET characteristics and hold significant potential to be further developed into a manufacturing process for making arrays of working FETs. In addition, using HfO_2-based high-*k* gate dielectrics, the mobility values of our FETs are expected to be further improved by at least 1 order of magnitude,[3] which is attributed to the dielectric screening effect.[51] The large arrays of such high-performance FETs produced by printing processes are expected to significantly facilitate the future scale-up electronic applications of few-layer MoS_2. In our future research, we will incorporate the top gates with sub-5 nm thick gate dielectrics into MoS_2 FETs in order to study the uniformity of other important FET parameters (*e.g.*, subthreshold slopes) and further explore the potential of our printing processes for manufacturing high-performance MoS_2-based electronic devices.

There are device applications requiring a more demanding control of the MoS_2 thickness. For example, optoelectronic applications usually need MoS_2 monolayers to obtain a large direct band gap.[6] For such applications, our printing approaches can potentially serve as a useful technique for transforming initial raw materials of few-layer MoS_2 into arrays of active device sites. These orderly formed MoS_2 flakes can be subsequently tailored through a series of postprinting processes to achieve a higher degree of uniformity in thickness and feature profile. For example, the laser-thinning technology with a self-termination mechanism recently developed by Castellanos-Gomez *et al.* could be used as a postprinting process for thinning as-printed MoS_2 flakes to increase the percentage yield of MoS_2 monolayers.[27] Furthermore, a postprinting lithography step (*e.g.*, photolithography and nanoimprint) followed by plasma etching can be easily implemented to trim as-printed MoS_2 flakes into functional nanopatterns with specific shapes.

CONCLUSION

In conclusion, we demonstrate a novel approach for producing ordered arrays of few-layer-MoS_2 device features. In this process, the relief structures are prepatterned onto a bulk MoS_2 film, which serves as a stamp for printing out orderly arranged MoS_2 pixel patterns over cm^2-scale areas on both pristine and plasma-charged SiO_2 substrates. MoS_2 pixels printed on plasma-charged substrates feature a higher degree of uniformity in pattern profiles and a narrower distribution of the MoS_2 flake thickness (*i.e.*, 3 ± 1.9 nm) in comparison with those printed on pristine substrates. This is attributed to the strong fringe field around the feature edges that is induced by plasma-introduced electric charges. We demonstrate that such printing approaches can be generalized for producing other emerging atomically layered nanostructures (*e.g.*, graphene nanoribbons). The printed MoS_2 flakes can be used to build working n-type FETs with excellent electronic properties (*i.e.*, $I_{ON}/I_{OFF} \approx 10^5$−$10^7$, mobility $\mu \approx 6$−44 cm^2/(V s)). Using additional plasma treatment processes, as-printed MoS_2 flakes can be doped to create p-type FETs as well as rectifying diodes. Finally, we systematically study the thickness-dependent characteristics of MoS_2 FETs and show that our printing processes can produce a high yield of electronic-grade MoS_2 flakes with an acceptable degree of uniformity in transport properties.

METHODS AND MATERIALS

Prepatterning of Bulk MoS_2 Stamps. To fabricate a bulk MoS_2 stamp, a piece of bulk MoS_2 is mechanically exfoliated from a MoS_2 source sample (SPI, Inc., size ~1 cm^2) and firmly attached onto a flexible copper tape. The exfoliated MoS_2 film has a fresh and pristine surface with total area of ~1 cm^2. To pattern

microscale relief features on the bulk MoS_2, a 1.4 μm thick photoresist layer is spun onto the MoS_2 surface and exposed on a Karl Suss MA6 photoaligner. The photomask used for this work bears periodic pillar patterns with pillar diameters ranging from 3 to 10 μm. After development, 100 nm thick Ti masks are formed on the MoS_2 surface by using electron-beam evaporation followed with lift-off in acetone. Afterward, the Ti mask patterns are etched onto the underlying MoS_2 using a SF_6-based RIE recipe (*i.e.*, SF_6 flow rate 20 sccm, pressure 20 mTorr, power 200 W) with an etching rate of ~100 nm/min. Finally, the Ti masks are removed by soaking the MoS_2 film in a diluted HF acid solution.

Transfer Printing of Prepatterned MoS_2 Flakes. Prepatterned few-layer MoS_2 flakes are transfer printed onto SiO_2/Si substrates that are cleaned by using the standard RCA process. To perform a transfer printing, a bulk MoS_2 stamp and a SiO_2/Si substrate are firmly pressed to each other by using a lab-made pressing system that can generate a gauge pressure up to 3 MPa for contact printing. To enhance the bonding strength between the MoS_2 flakes and the SiO_2 surface, an O_2-based plasma recipe (*i.e.*, O_2 flow rate 50 sccm, pressure 25 mTorr, power 100 W, time duration 2 min) is used to treat the SiO_2 surface before the printing step. Such a plasma treatment is expected to introduce uniformly distributed electric charges on the SiO_2 surface that can provide additional electrostatic attractive stress for exfoliating prepatterned few-layer MoS_2 flakes from the bulk stamp.[32] After the printing process, the printed MoS_2 patterns are imaged by using a scanning electron microscope in secondary-electron and backscattered modes as well as an optical microscope. An atomic force microscope is employed to measure the thickness of printed MoS_2 features in the tapping mode. In addition, an X-ray energy dispersive spectrometer integrated with a SEM system is used to confirm the presence of MoS_2 features within the printed areas.

Fabrication of Field-Effect Transistors Using Printed MoS_2 Flakes. To fabricate back-gated MoS_2 FETs, the metallic drain/source contacts (5 nm Ti/55 nm Au) are fabricated by photolithography or electron-beam lithography followed by metal deposition and lift-off. In particular, photolithography is used for fabricating FETs based on the inner flakes of MoS_2 pixels, and EBL is specifically used for fabricating FETs based on the outer edge ribbons of MoS_2 pixels. Finally, another metallic contact is made onto the p^+-Si substrate, which serves as a back gate contact. The device characteristic curves of FETs are measured using an Agilent-4145B semiconductor parameter analyzer.

Plasma-Assisted Transfer Printing of Prepatterned Graphene Nanoribbons. First, a highly oriented pyrolytic graphite stamp (SPI, Inc.) is prepatterned with 100 nm half-pitch, 100 nm deep relief gratings, as shown in Figure 6(a). Such grating features are replicated from a master mold (Nanonex, Inc.) by using thermal nanoimprint lithography (T-NIL) followed by O_2-based plasma etching.[46] The T-NIL process was performed on a Specac thermal pressing tool equipped with a cooling-water system. The fabricated HOPG stamp is subsequently used to stamp out graphene nanoribbons onto plasma-charged SiO_2 substrates. The plasma-assisted printing process performed here is the same as the process used for printing microscale MoS_2 pixel arrays.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Additional SEM images of MoS_2 flake arrays printed onto pristine SiO_2 substrates that were captured over large areas (Figure S1); additional SEM images of MoS_2 pixel flakes printed onto plasma-charged SiO_2 substrates (Figure S2); EDS spectra of outer edge ribbons and inner flakes of printed MoS_2 pixels (Figure S3); optical micrographs of MoS_2 pixel flakes printed on plasma-charged SiO_2 substrates (Figure S4); finite element analysis for simulating electric field around the edge ribbon of a MoS_2 pixel and calculating the effective gate capacitance of edge ribbon-based FETs (C_g) (Figure S5); $I_{DS}-V_G$ characteristic curves of 14 back-gated FETs made from the inner flakes of MoS_2 pixels printed on a single substrate (Figure S6). This material is available free of charge *via* the Internet at http://pubs.acs.org.

Acknowledgment. This work is supported in part by NSF grant CMMI-1232883, in part by the new faculty start-up fund from the Department of Mechanical Engineering, University of Michigan, and in part by the Open-Lab Program (Project No. 12ZD05) of the Key Laboratory of Nanodevices and Applications, Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO), Chinese Academy of Sciences. The authors would like to thank the staff of the Univeristy of Michigan's North Campus Electron Microbeam Analysis Laboratory and NSF grants (DMR-0320740 and 0315633) for providing the support of SEM imaging and EDS characterization; the staff of the University of Michigan's Lurie Nanofabrication Facility for providing the support of AFM imaging and device fabrication and an NSF grant (ECCS-0922972) for providing the support of electron-beam lithography; the staff of Nanofabrication Facility and Platform for Characterization & Test, SINANO, for additional process verification; and Prof. A. Boehman and Prof. P. S. Reddy for their precious advice in revising the manuscript. H.N. would like to thank Korea Institute of Energy Technology Evaluation and Planning for providing overseas scholarship funds.

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